POLITECNICO DI MILANO





Distributed Synchronization Algorithms for Wireless Sensor Networks

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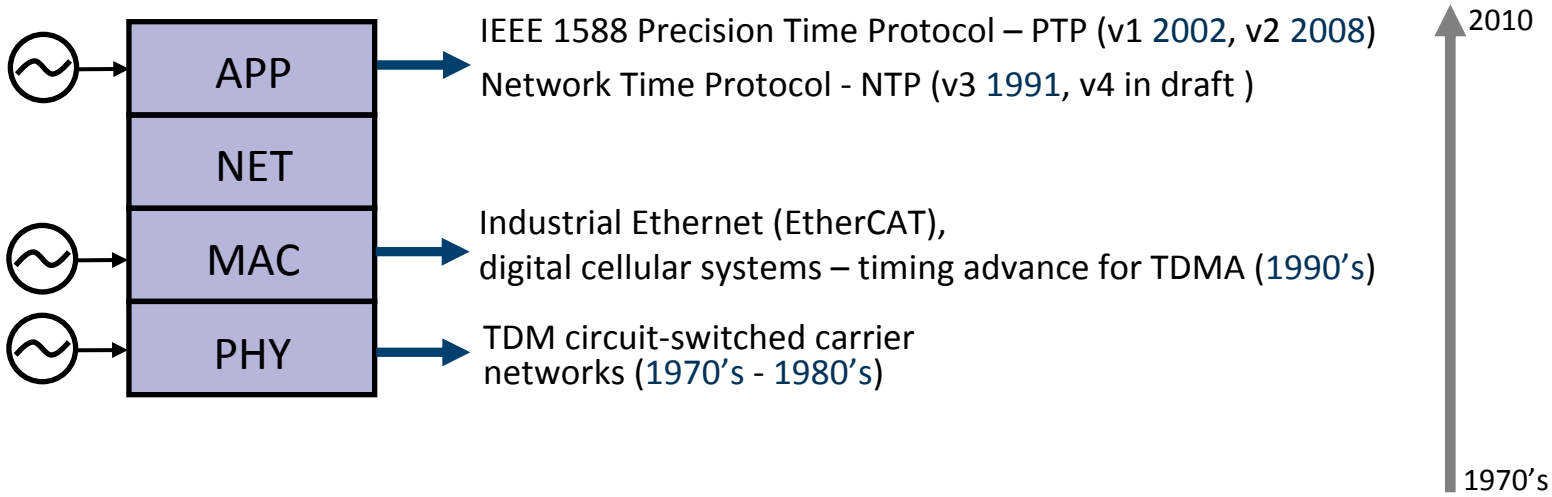
Outline

- Motivation
- Synchronization at the physical layer
- Synchronization at the MAC layer
- Conclusions

Network Synchronization

Synchronization is the simplest form of cooperation and enables more complex cooperative tasks

- Communication *Networks*: synchronization at different layers



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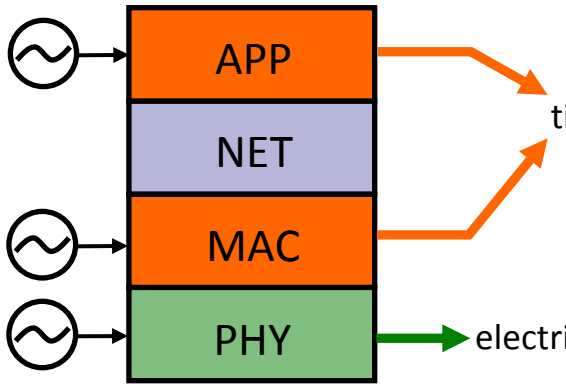

timing packets:
- *Software* PLL (linear clock control)
- Kalman tracking
- estimation of clock parameters (phase/frequency/drift)
- other (e.g., nonlinear clock correction)

electrical/RF signals:
- Analogue Phase-locked Loop (APLL)
- (All) Digital PLL (DPLL)
- analogue/digital Frequency-locked Loop (FLL)

Motivation

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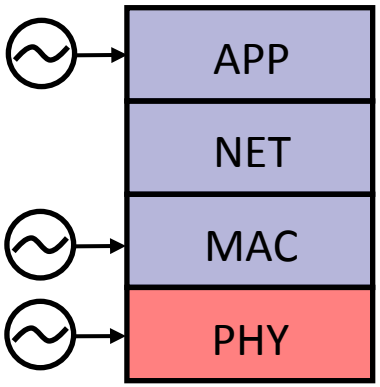
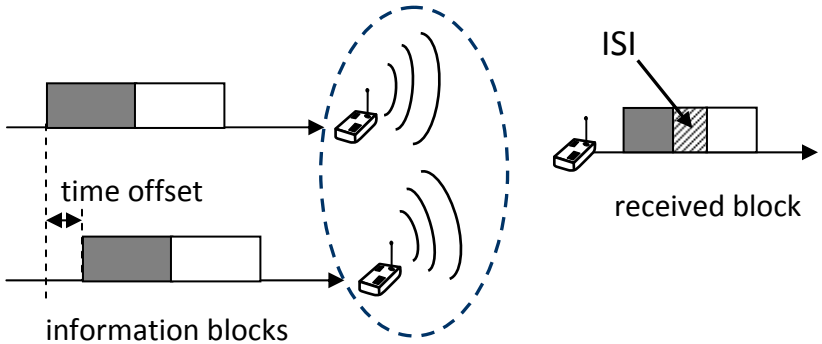
- *Wireless Sensor* Networks:
  synchronization at different layers



physical: cooperative communication

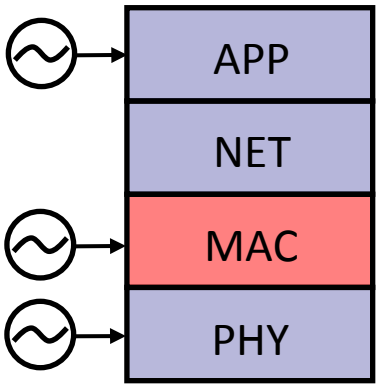


distributed space-time code

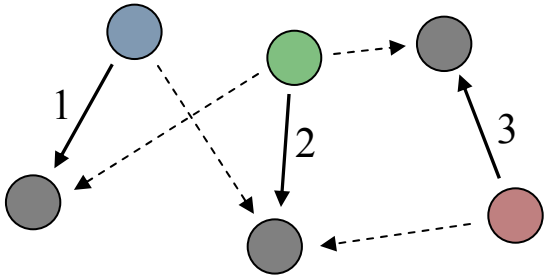
Motivation

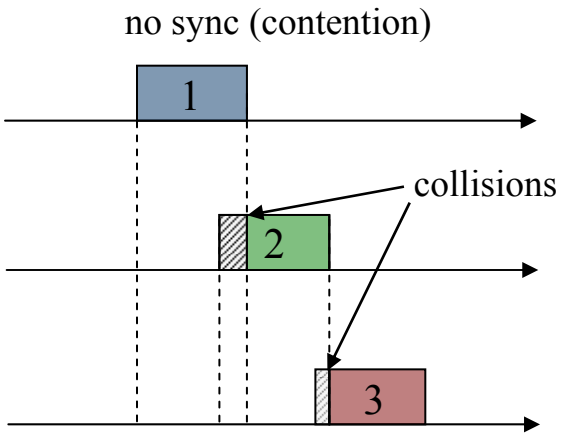
Synchronization is the simplest form of cooperation and enables more complex cooperative tasks

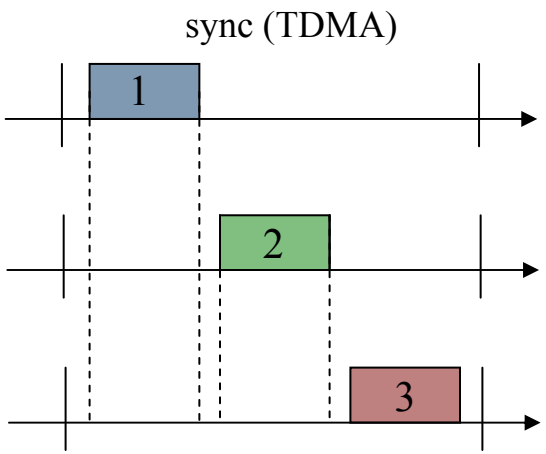
- *Wireless Sensor* Networks: synchronization at different layers



MAC: coordinated medium access



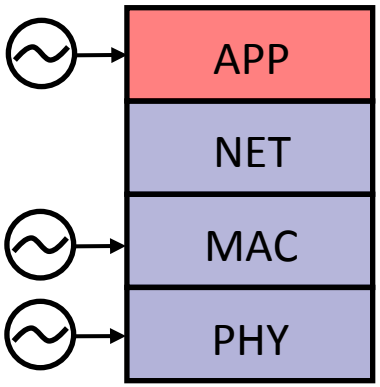




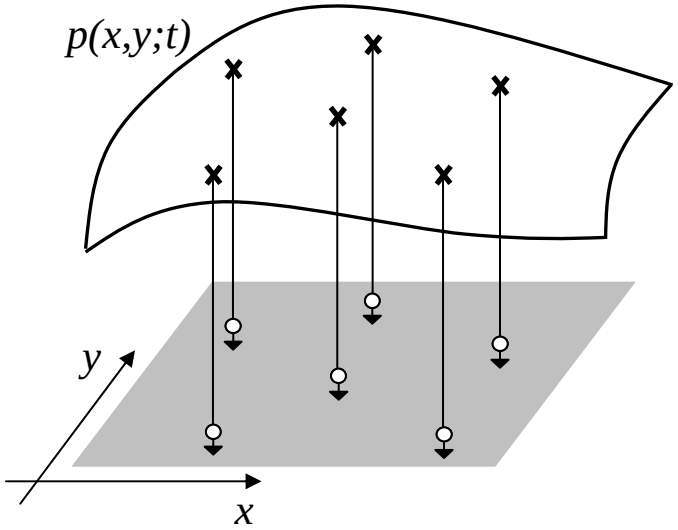
Motivation

Synchronization is the simplest form of cooperation and enables more complex cooperative tasks

- *Wireless Sensor* Networks:
  synchronization at different layers



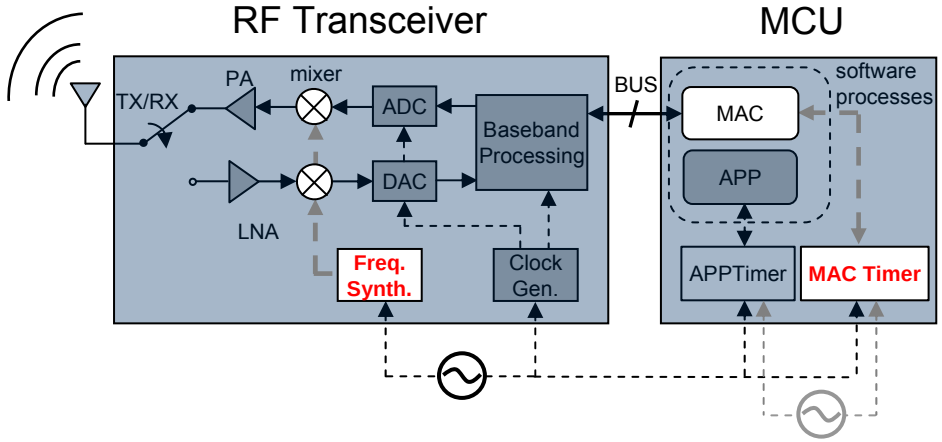
application: distributed sensing

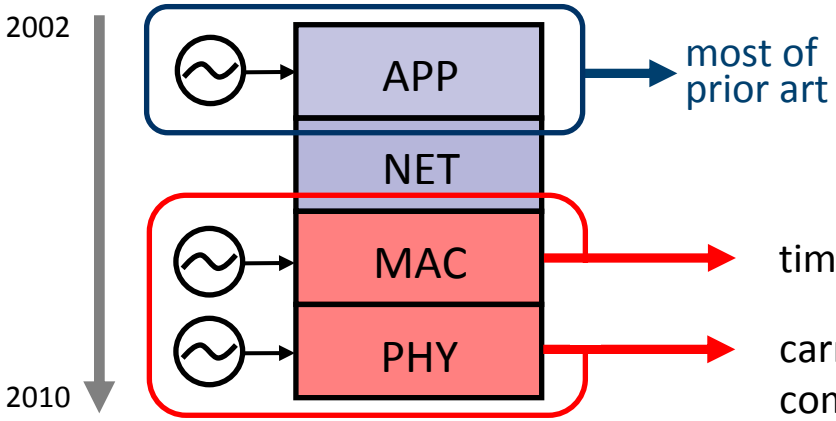


Focus of Major Research Topic

Synchronization is the simplest form of cooperation and enables more complex cooperative tasks

- *Wireless Sensor* Networks: synchronization at different layers



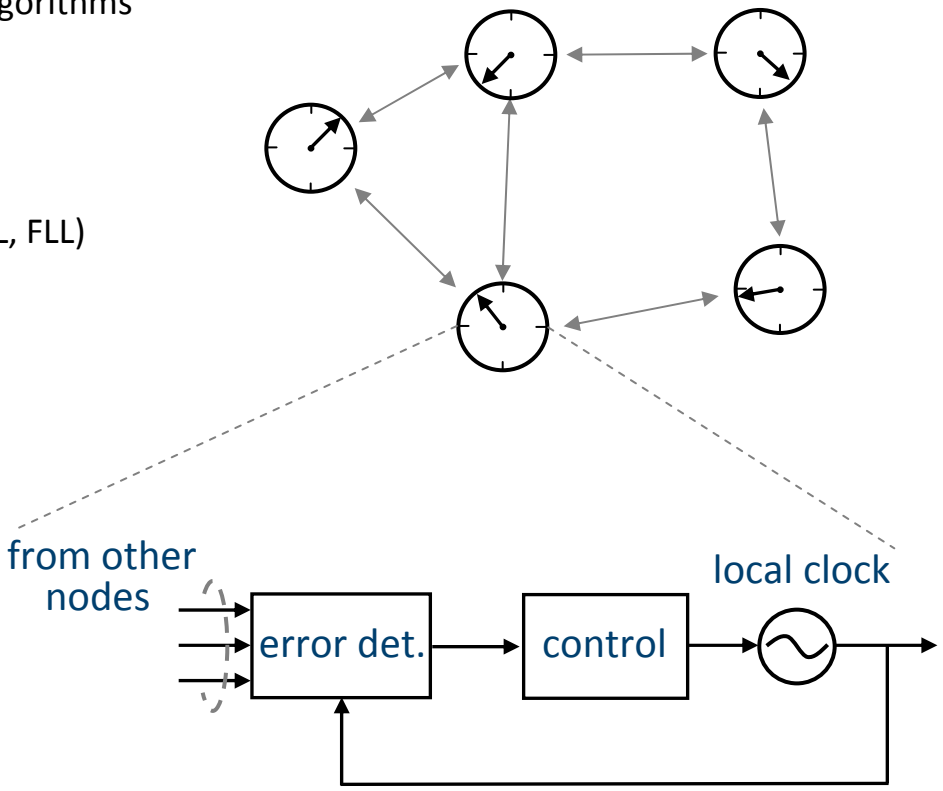


Approach: Clock Control

- Prior Art:
  - *estimation* of clock parameters [Kumar08][Estrin04]
  - distributed agreement (consensus) algorithms [Simeone07][Schenato09]
- Our approach:
  control of the local clock
  via Phase and Frequency-Locked Loops (PLL, FLL)

PLL is the classical approach for wired networks (TDM, NTP, PTP)

what about wireless ?



Approach: Clock Control

- Prior Art:
  - *estimation* of clock parameters
  - distributed agreement algorithms
- Our approach:
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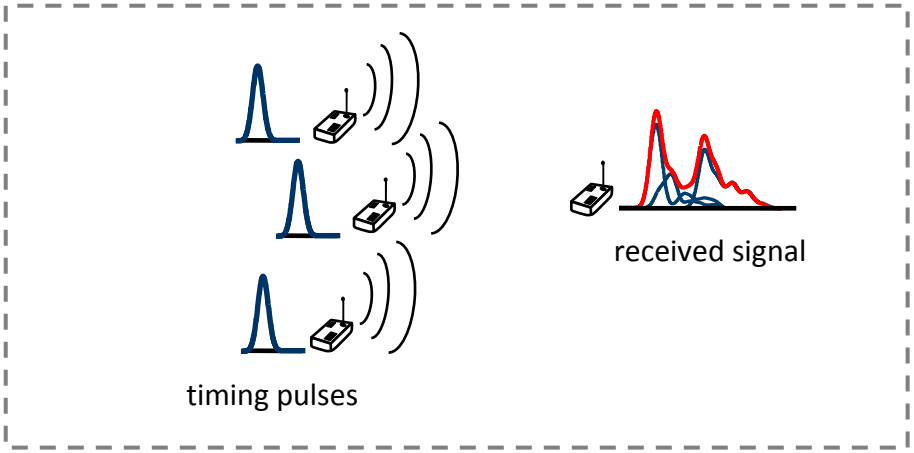
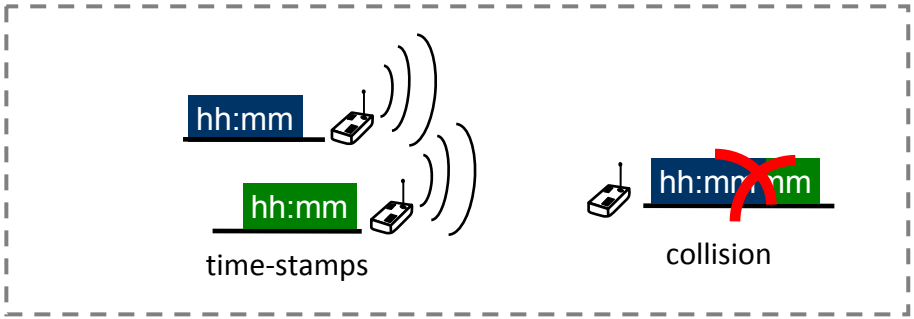
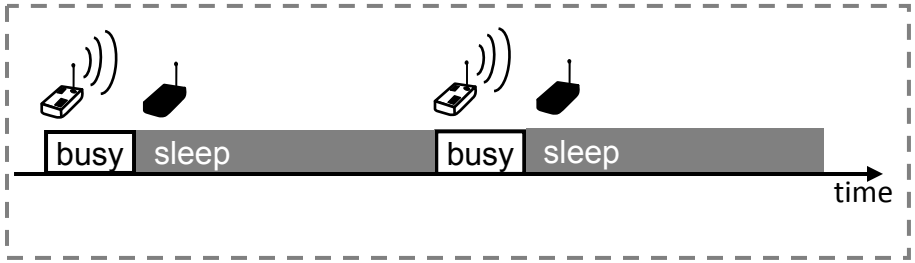
  via Phase and Frequency-Locked Loops (PLL, FLL)

- Challenges:
  - superposition of radio signals
  - packet collisions
  - energy constraints (low duty cycles)

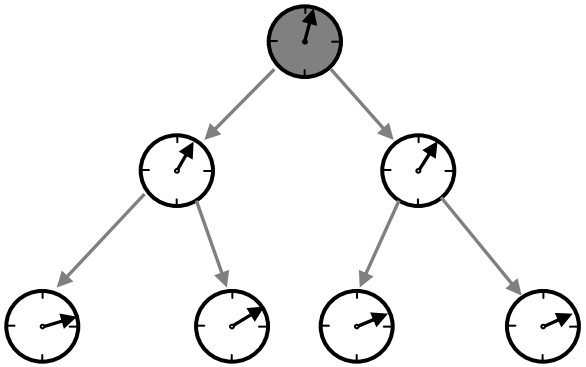




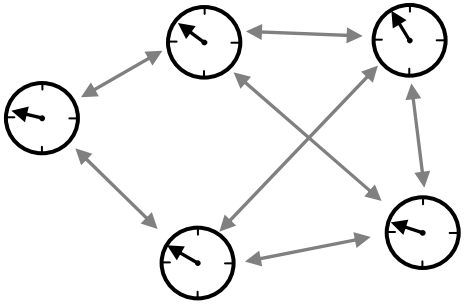


Approach: Sync Topologies

master-slave (MS): hierarchical



mutually coupled (MC): peer-to-peer

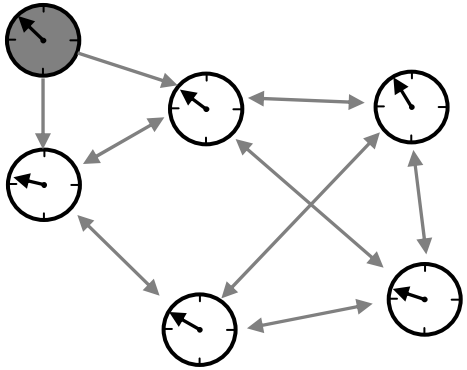


- WSN offer wider flexibility in sync architecture design
- Prior Art:

  specific tools for each sync topology, e.g.
  - MS: linear regression (FTSP [Maróti04])
  - MC: distributed consensus (ATS [Schenato09])
- Our approach:

  PLL/FLL as a *distributed* clock control tool suitable for *any* sync topology

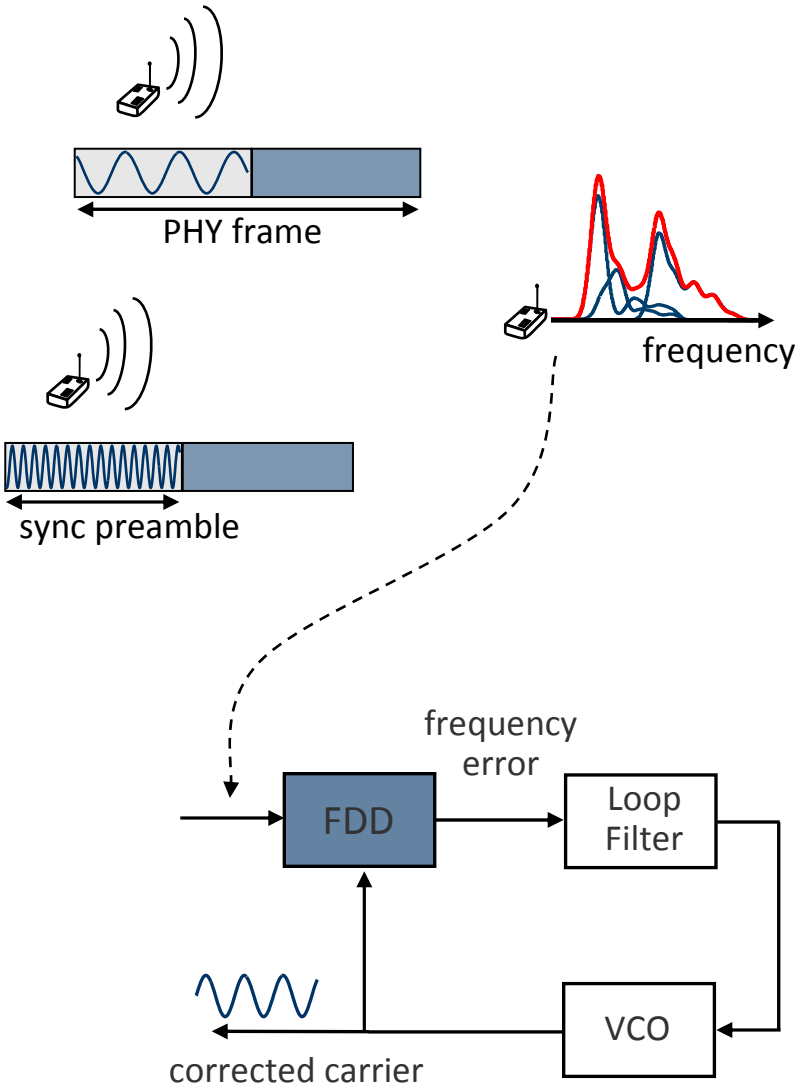
hybrid



Outline

- Motivation
- Synchronization at the physical layer
  - distributed compensation of Carrier Frequency Offsets (CFO)
- Synchronization at the MAC layer
- Conclusions

Distributed CFO Correction

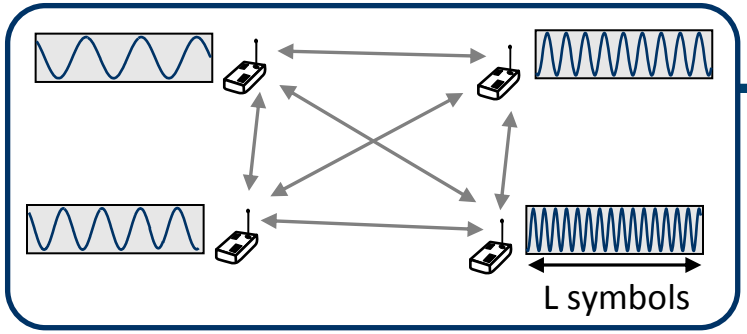


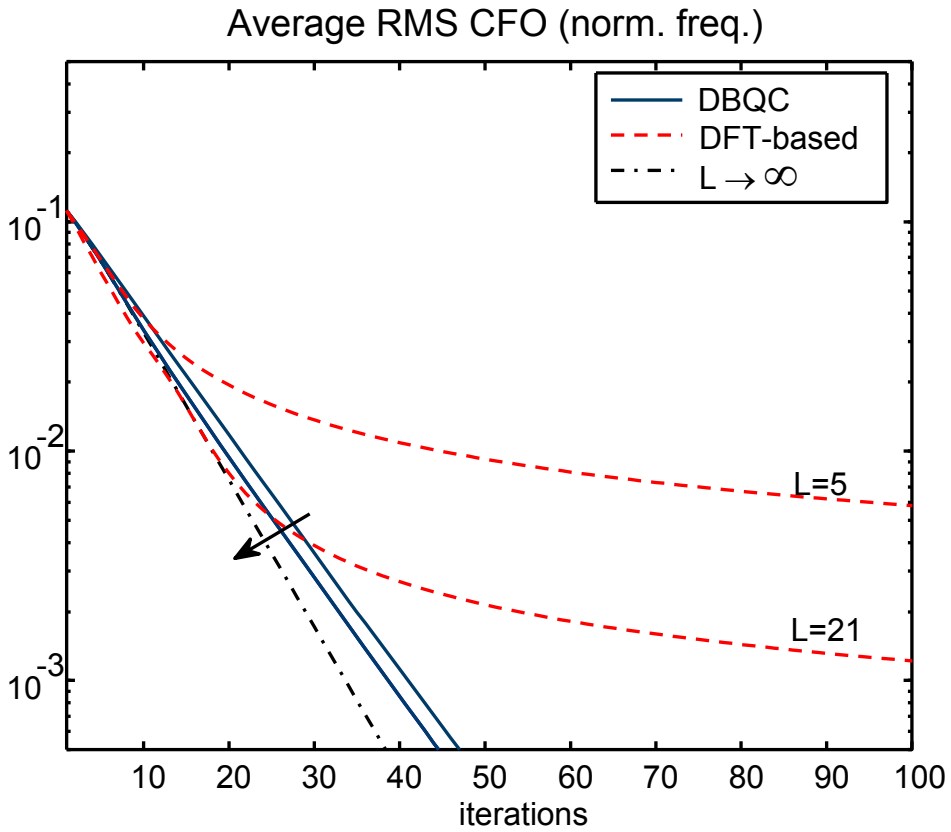
- Sync preamble for CFO estimation
- CFO correction via *distributed-FLL* (D-FLL)
- design of novel Frequency Difference Detector (FDD)
  - *superposition* of preamble signals
  - based on sample auto-correlation
  - nonlinear characteristic
- analysis:
  - frequency *acquisition* (stability and conv. speed)
  - steady-state sync *accuracy*

Frequency Acquisition

- frequency acquisition
  - FDD locking range
  - stability conditions (MC networks)
    - connectivity
    - mutual interference

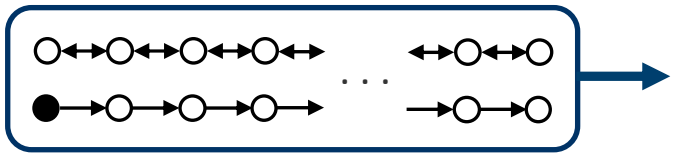
- comparison with DFT-based FDD for a simple MC network



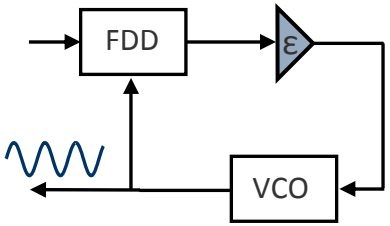


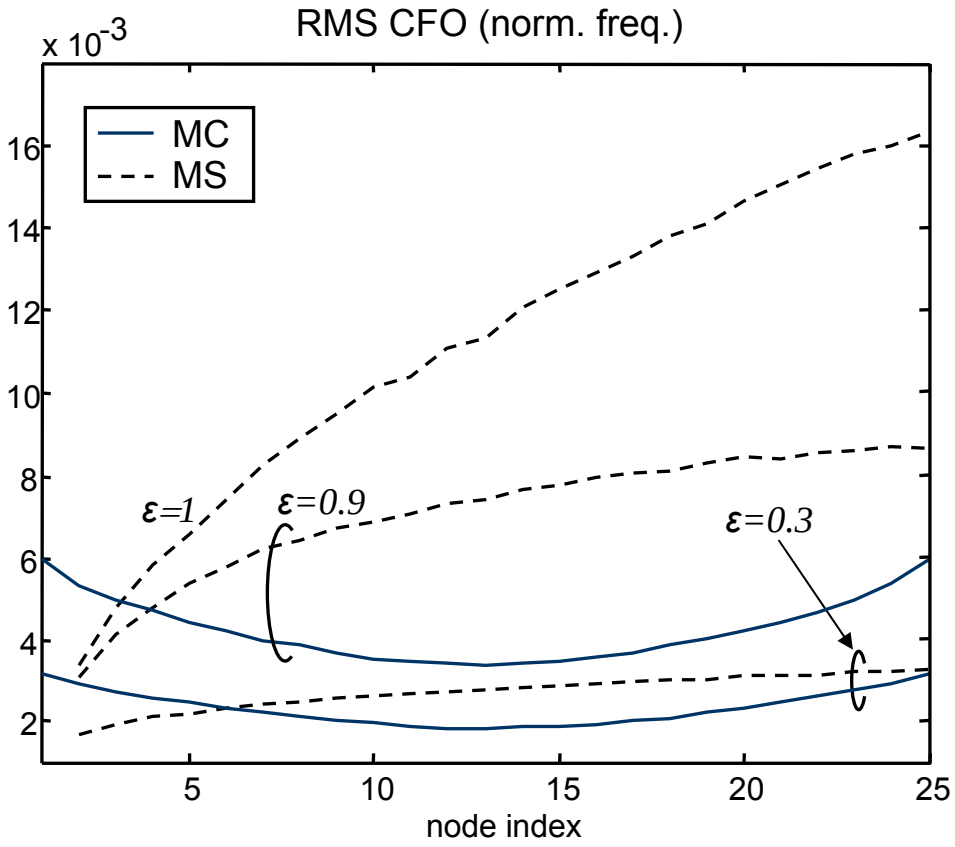
Frequency Tracking

- Steady-state sync accuracy
  - channel noise and frequency instability (WFM)
  - MC and MS topologies
- residual CFO distribution in a MC and MS line network



- FLL bandwidth tuned via loop gain ε





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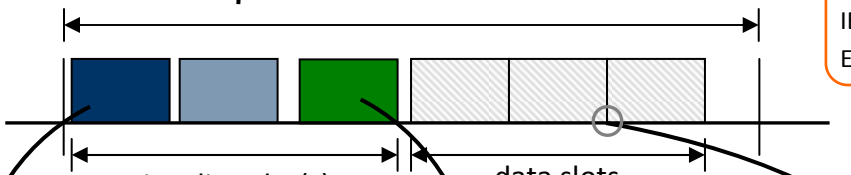
Super-frame structure

General SF structure

for a slotted-access MAC layer :

super-frame length = sync update period

IEEE 802.15.4/e (ZigBee/SP100)
IEEE 802.11 (Wi-Fi)
ECMA 368 (WiMedia)



need for *time sync*: slot timing

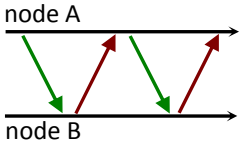
Time information:

- pulse (frame sync seq.)

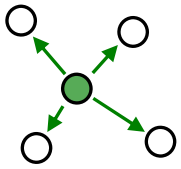
- time-stamp

→ *access protocols for signaling slots*

NTP/PTP, others: handshakes



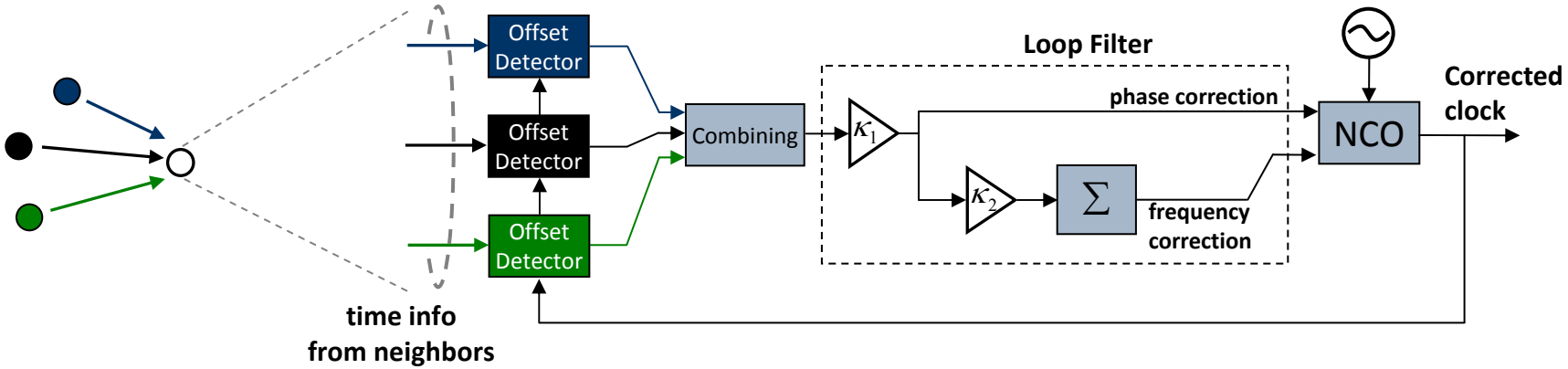
our case: broadcast



→ *no timing handshakes*

Type 2 PLL

Each node employs time info to control the local clock via a PLL:



Analysis of *distributed* PLL:

- time sync *acquisition* (stability and conv. speed)
- steady-state accuracy:
  - *stable* clocks : frequency is constant bw updates
  - *unstable* clocks : frequency changes bw updates

Impact of topology
- MC
- MS

Choice of loop parameters:
- loop gain κ_1
- damping $\zeta(\kappa_1, \kappa_2)$

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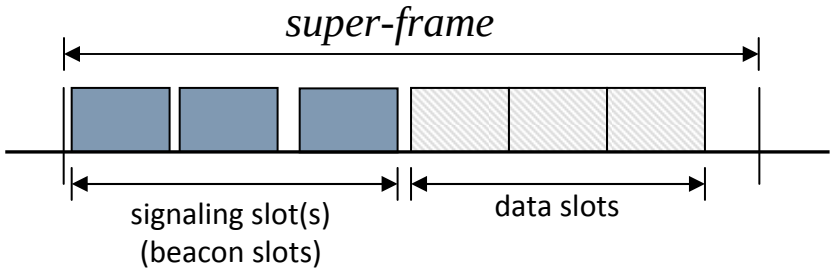
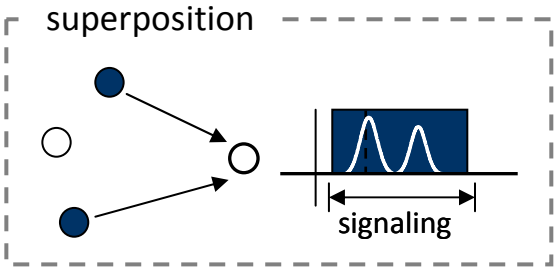
Time Sync Acquisition



Time information:

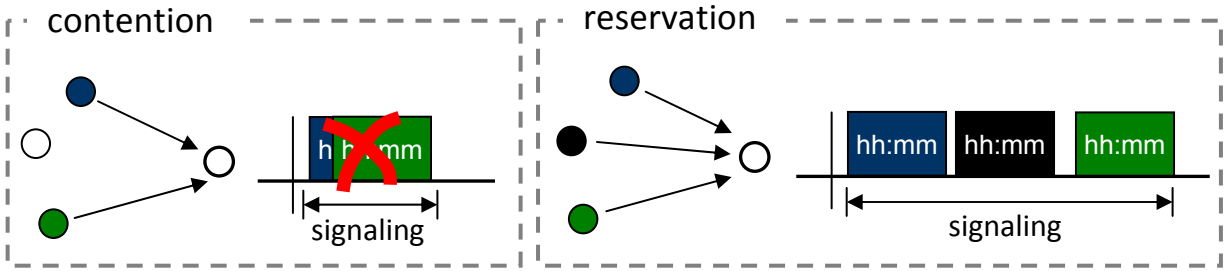
- pulse (frame sync word)

  → *superposition* of pulses

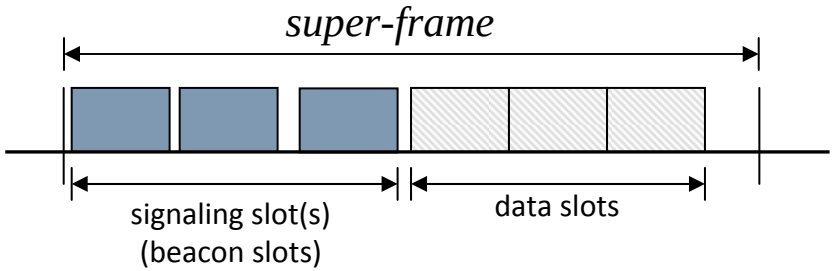


- time-stamp

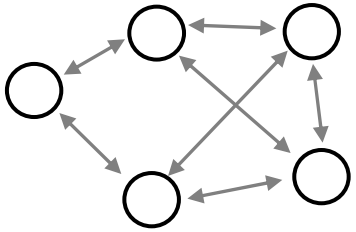
  → *contention* or *reservation*-based transmission



Time Sync Acquisition - Results

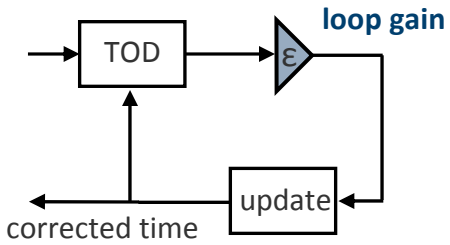


- acquisition trivial for MS → analysis focused on *MC networks*
- *superposition* and *contention:*
  - almost sure convergence condition : convergence *in the mean*
- *reservation :*
  - overhead of signaling slots

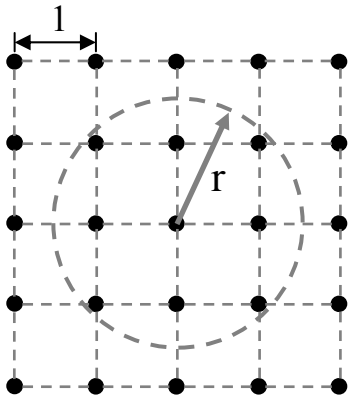


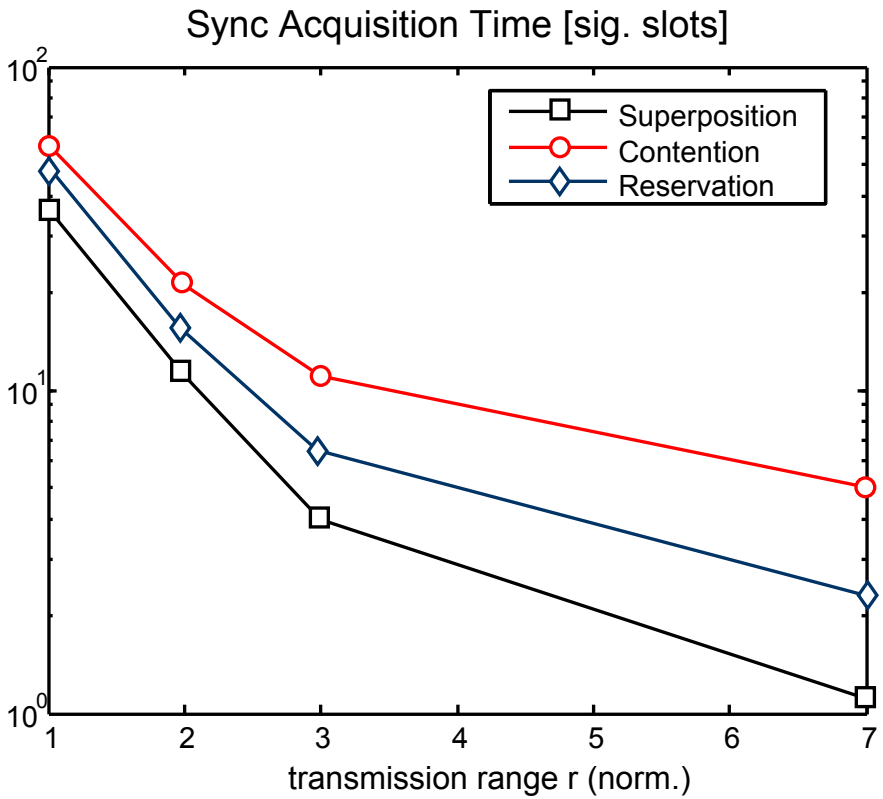
Time Sync Acquisition - Results

- Hp: clocks are frequency synchronous
  - Type 1 PLL for time (phase) sync



- $0 < \varepsilon < 1$ ensures stability
- numerical optimization of loop gain ε for a given square lattice topology:





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  - Steady-state sync accuracy
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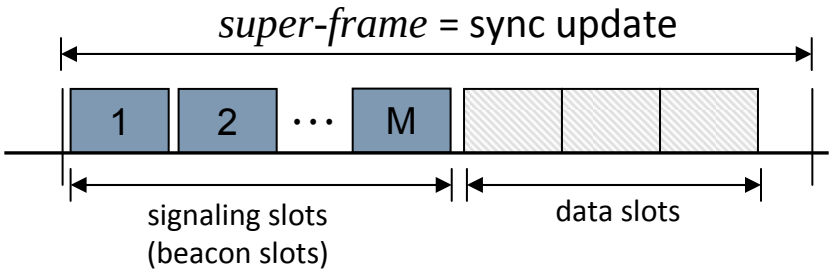
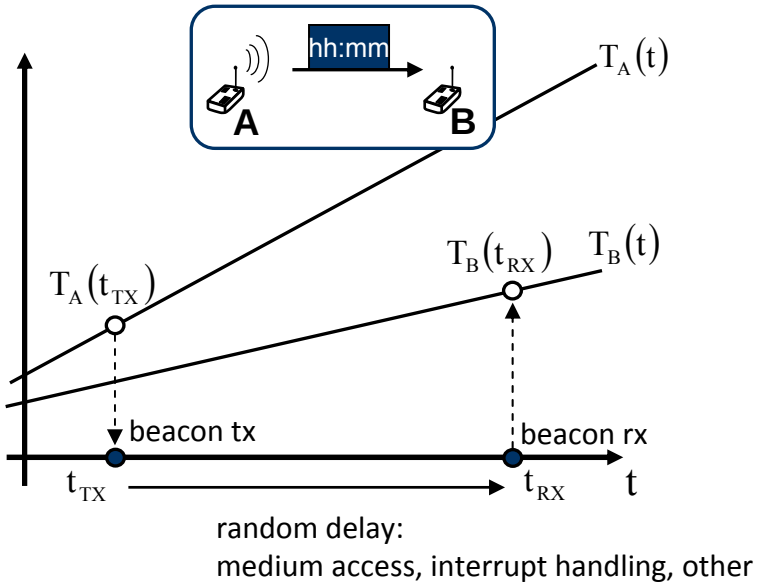
Synchronization Accuracy

- TDMA MAC protocol
  - *reservation*-based signaling
- Hp: clk frequency is *stable*
  - linear clock model

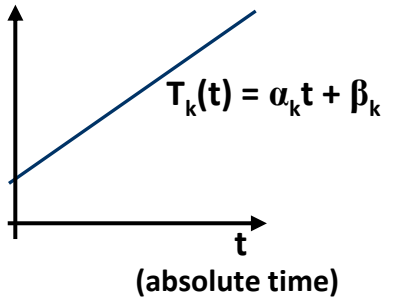


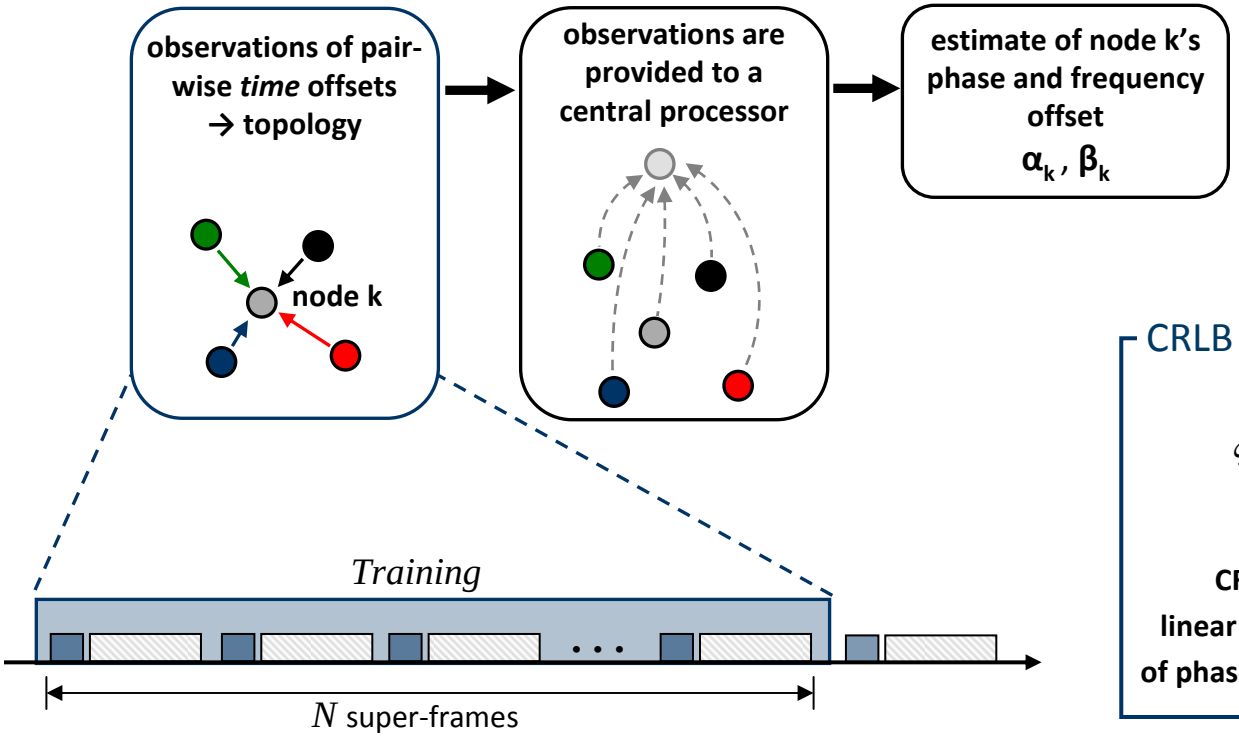
- sync accuracy depends on *pair-wise offset* estimation errors.
  - delivery delays
  - clock precision (quantization)
- network sync posed as a (distributed) linear regression problem
  - distributed type 2 PLL
  - → distributed linear regression (DLR)
  - → *Cramér–Rao lower bound*



Cramér–Rao Lower Bound

- CRLB: lower bound to clock parameter estimation error
  - linear clock model : estimate phase and frequency
  - time offset observations from signaling slots of subsequent super-frames
  - *centralized block*-estimation model:





CRLB for a general topology

$$\xi^2_{p,f} \geq \rho_{p,f} \frac{1}{K} \sum_{i=1}^{K_u} \frac{1}{\mu_i}$$

CRLB for linear regression of phase/frequency

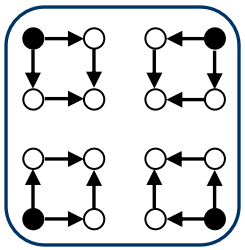
sync network architecture

CRLB : MS Vs MC

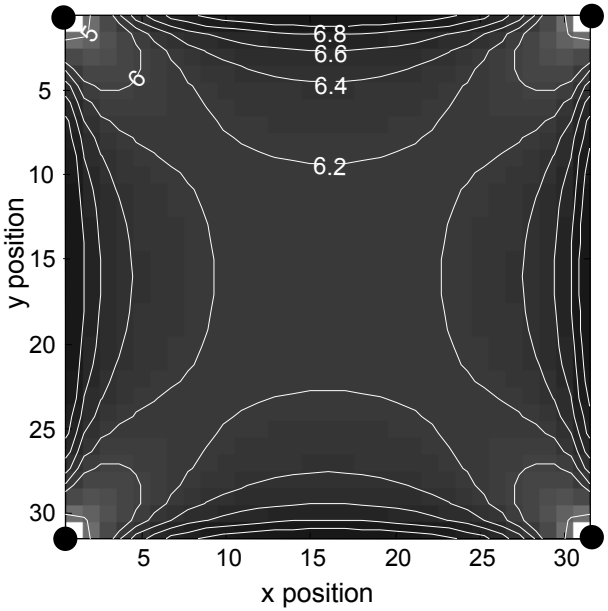
- Cramér–Rao lower bound for general sync architectures (MS, MC, hybrid)
  - MC: error distributed almost uniformly
  - MS: error distributed inhomogeneously - accuracy degrades rapidly moving away from masters

- CRLB for 2D 30x30 square lattice deployment (in μs)

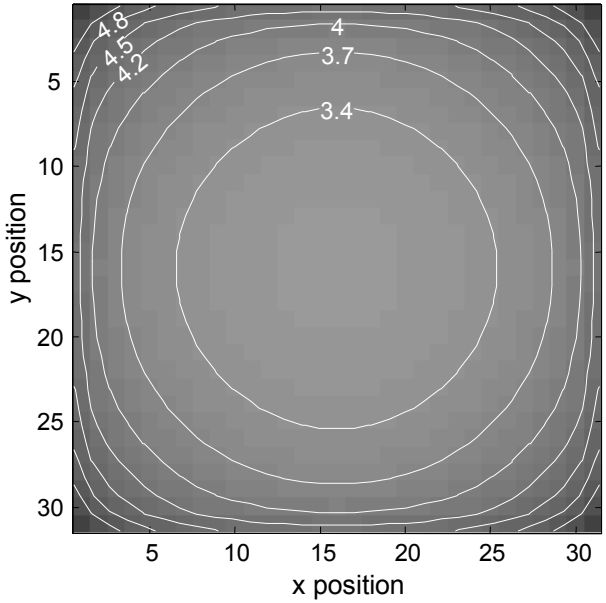
  (Gaussian offset measurement error with 10μs std dev, N=10)

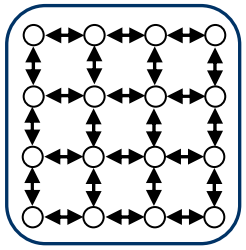


MS architecture



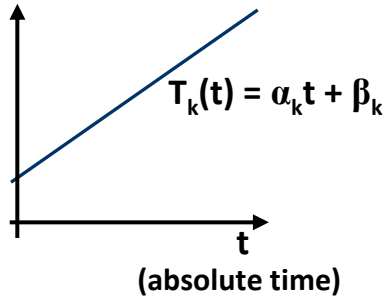
MC architecture

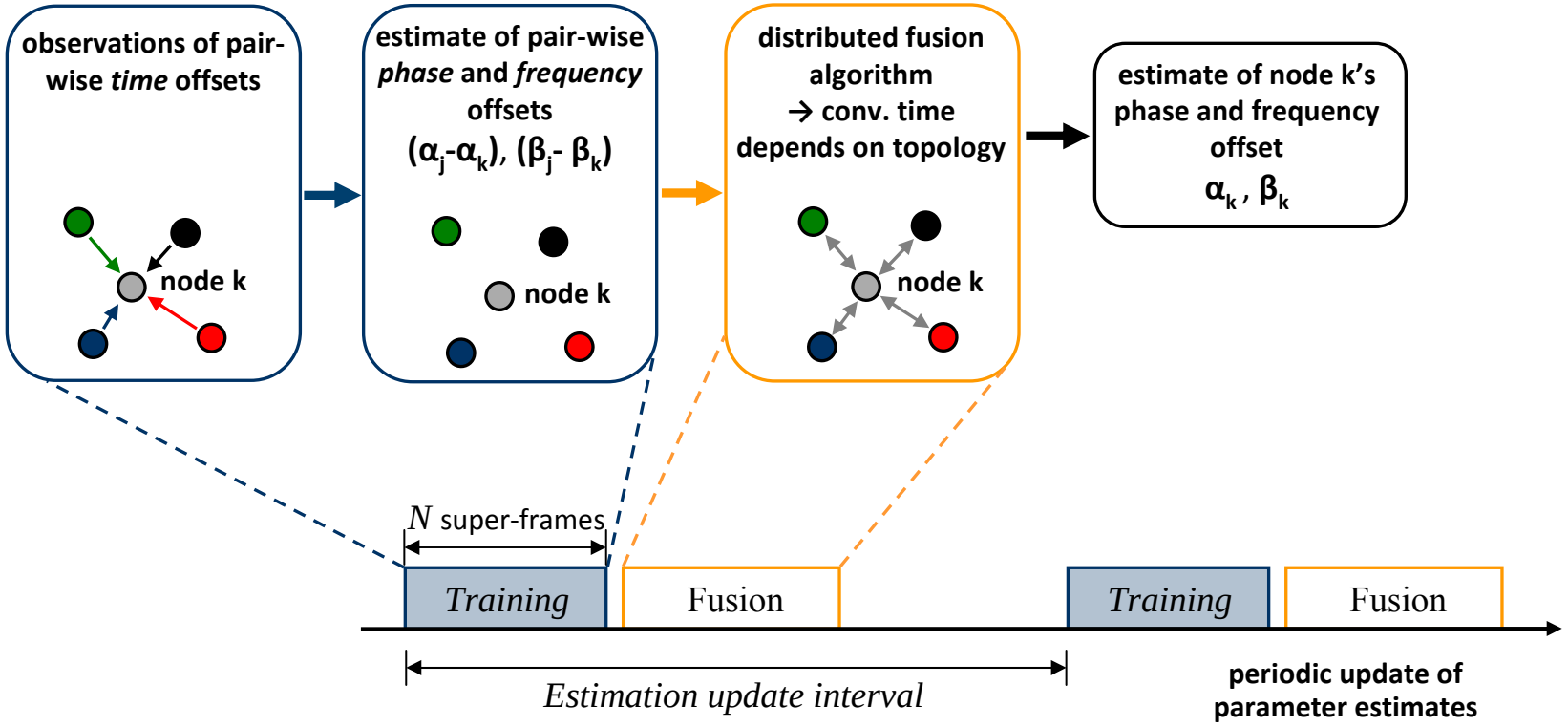




Distributed Linear Regression

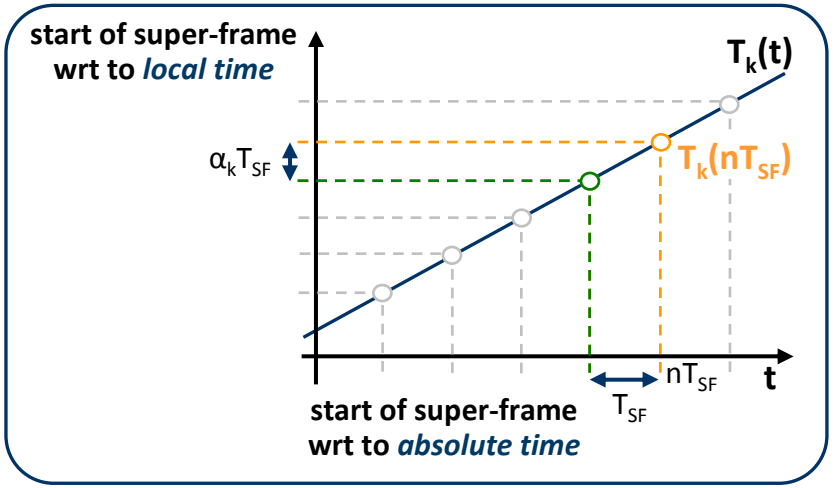
- Design of *Distributed linear regression* (DLR) algorithm
  - linear clock model : estimate phase and frequency
  - time translation : $t = (T_k(t) - \beta_k)/\alpha_k$
  - signaling slots employed for training and ***distributed fusion***

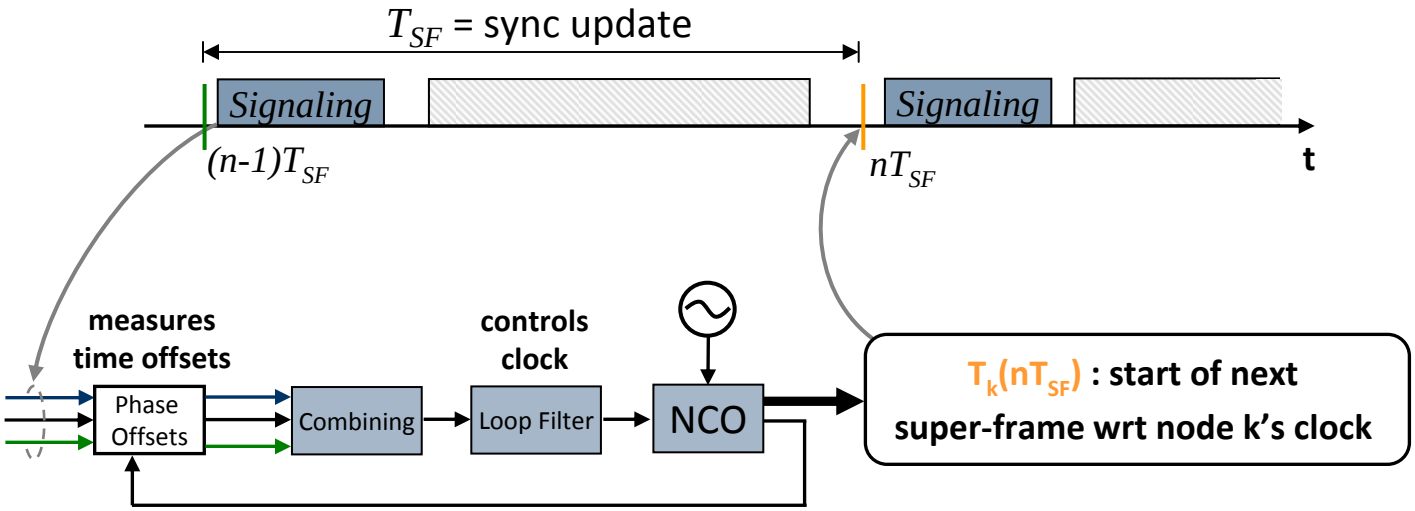




Type 2 PLL

- PLL clock control
  - linear clock model → linear clock control
  - PI (type 2) controller: phase and frequency control
  - provides a prediction of the start time of next super-frame ***wrt local clock***





Lessons Learned

- DLR: closed-form sync accuracy for general networks
- PLL: closed-form sync accuracy for regular MC networks
- *Effective* samples for PLL algorithms [Mengali94]

$$N_{eff} = \frac{2}{\frac{\kappa_1}{2}\left(1+\frac{\kappa_2}{\kappa_1}\right)}$$

- *Regular* topology*: ring network*
  - CRB accuracy limit

$$\xi^2_{CRB} \simeq \frac{2\sigma_w^2}{N_{eff}} \frac{1}{\mu_2}$$

  - DLR accuracy

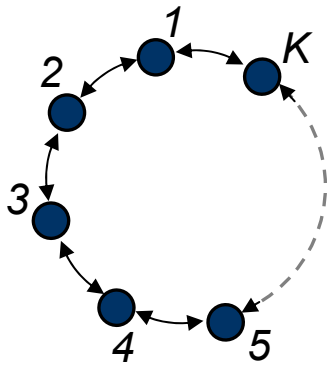
$$\xi^2_{DLR} \simeq \frac{4d\sigma_w^2}{N_{eff}} \frac{1}{\mu_2^2}$$

  - PLL accuracy

$$\xi^2_{PLL} \simeq \frac{4d\sigma_w^2}{N_{eff}} \frac{1}{\mu_2^2} \frac{1}{1+4\zeta^2}$$

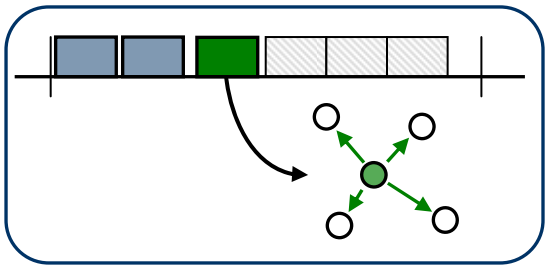
better connectivity improves accuracy

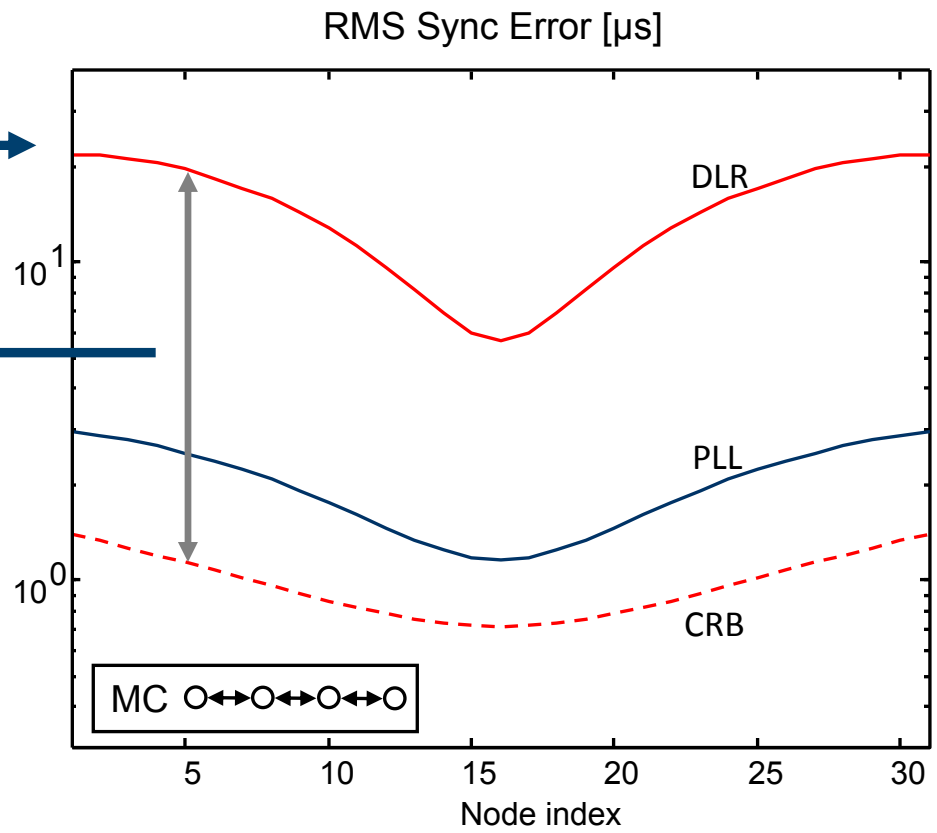
improved noise filtering



Accuracy of MC Networks

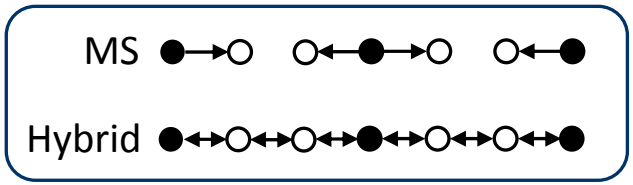
- Accuracy of practical algorithms over MC networks
- line network of 31 nodes, N=1000
- sub-optimality of both PLL and DLR wrt CRB
  - price to pay for *broadcast* signaling



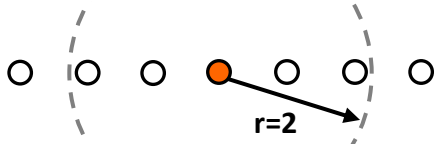


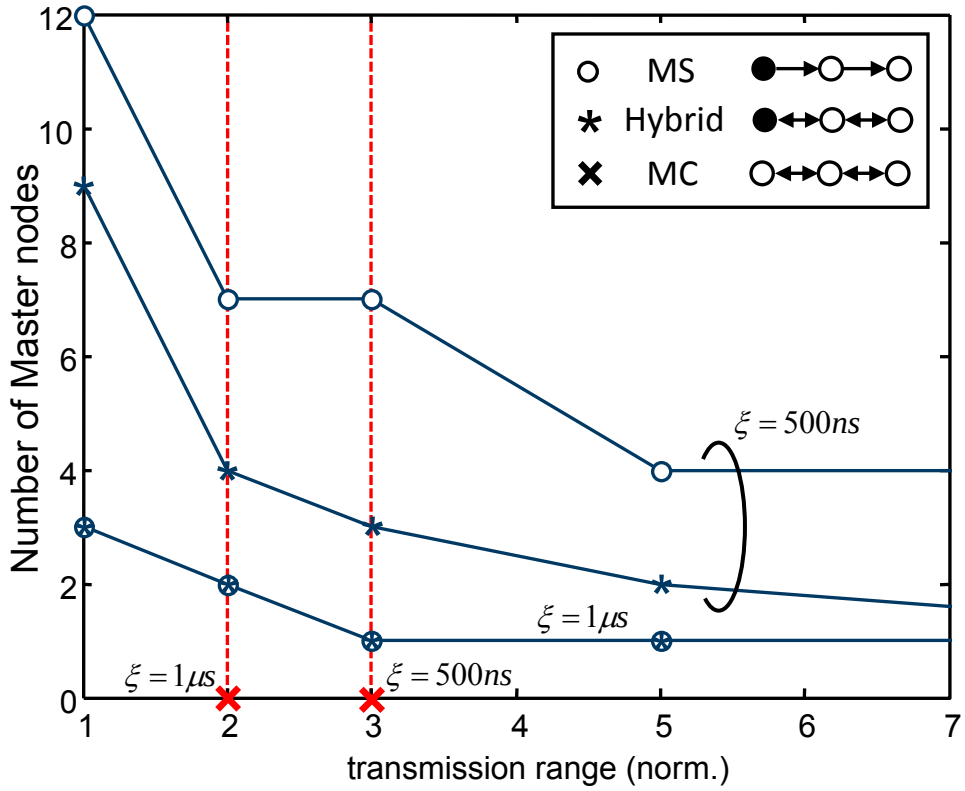
PLL: MC Vs MS

- Fix a desired time (phase) sync accuracy ξ
  - MC: accuracy improves *increasing transmission range*
  - MS/Hybrid: accuracy improves increasing transmission range or *master node density*



- MS/Hybrid: for a given transmission range, *how many master nodes do I need ?*
- line network of 31 nodes, N=1000
- MC accuracy rapidly improves with transmission range



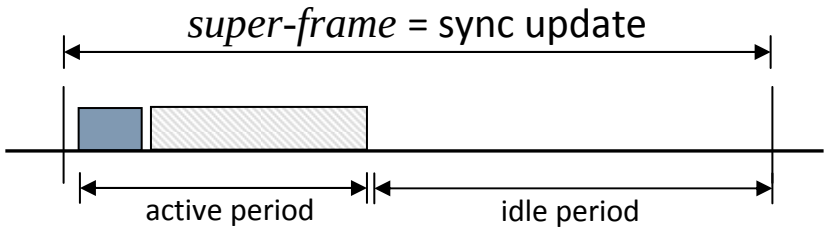


Outline

- Motivation
- Synchronization at the physical layer
- Synchronization at the MAC layer
  - Convergence rate of distributed sync algorithms
  - Steady-state sync accuracy
  - Sync tracking with low duty-cycles
- Conclusions

Sync Tracking with Low Duty-Cycles

- TDMA MAC protocol
  - *reservation*-based signaling
- low duty cycle → infrequent sync updates
  - clock is *unstable*: temp. changes



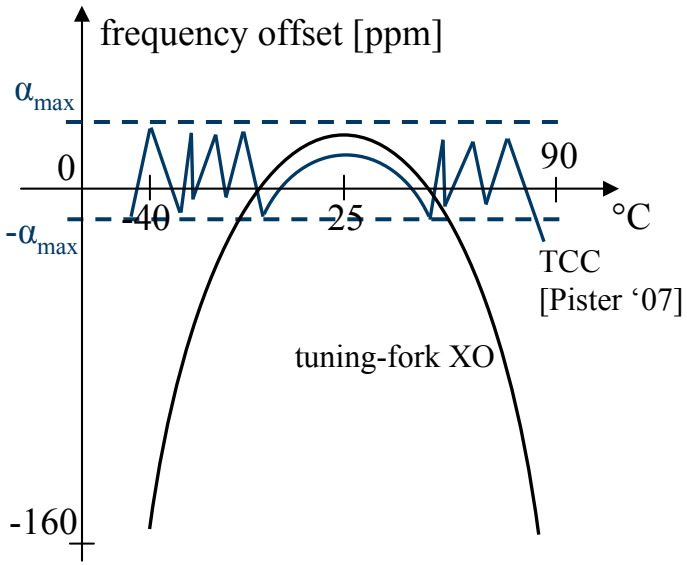
- *current solution*: static temp. compensation (Temp. Compensated Clock - TCC)
- achievable accuracy (lower bound for MS)

MS ●→○

$$\xi = 2\alpha_{\max} T_{SF} + \delta$$

residual frequ. offset

phase offset estimation accuracy



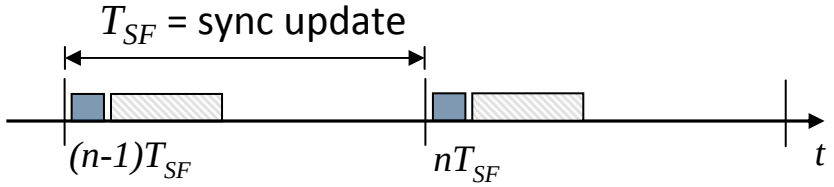
Model of an Unstable Clock

- Hp: clock frequency is the sum of two indep. random processes

$$\alpha(nT_{SF}) = \bar{\alpha} + v(nT_{SF}) + w(nT_{SF})$$

random walk (RWFM) — white noise (WFM)

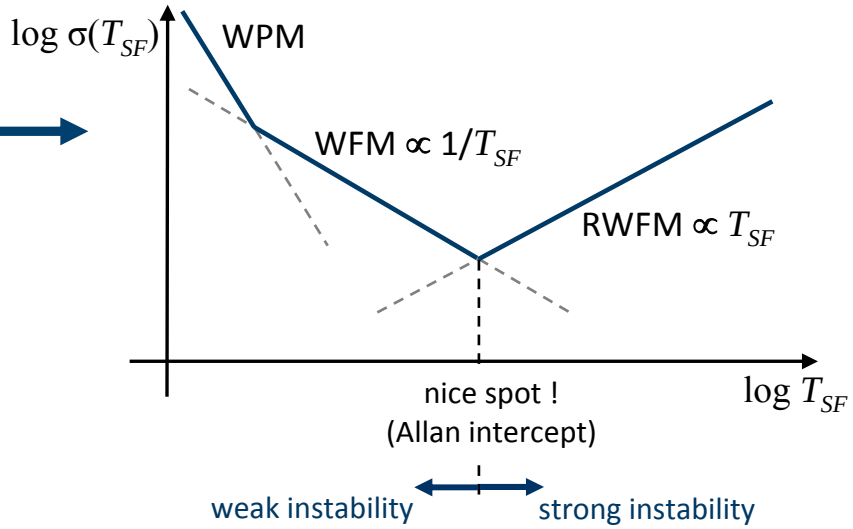
  - WFM: noise within the oscillator
  - RWFM: temperature changes, mechanical shocks and vibrations



- Allan Variance: a measure of frequency stability

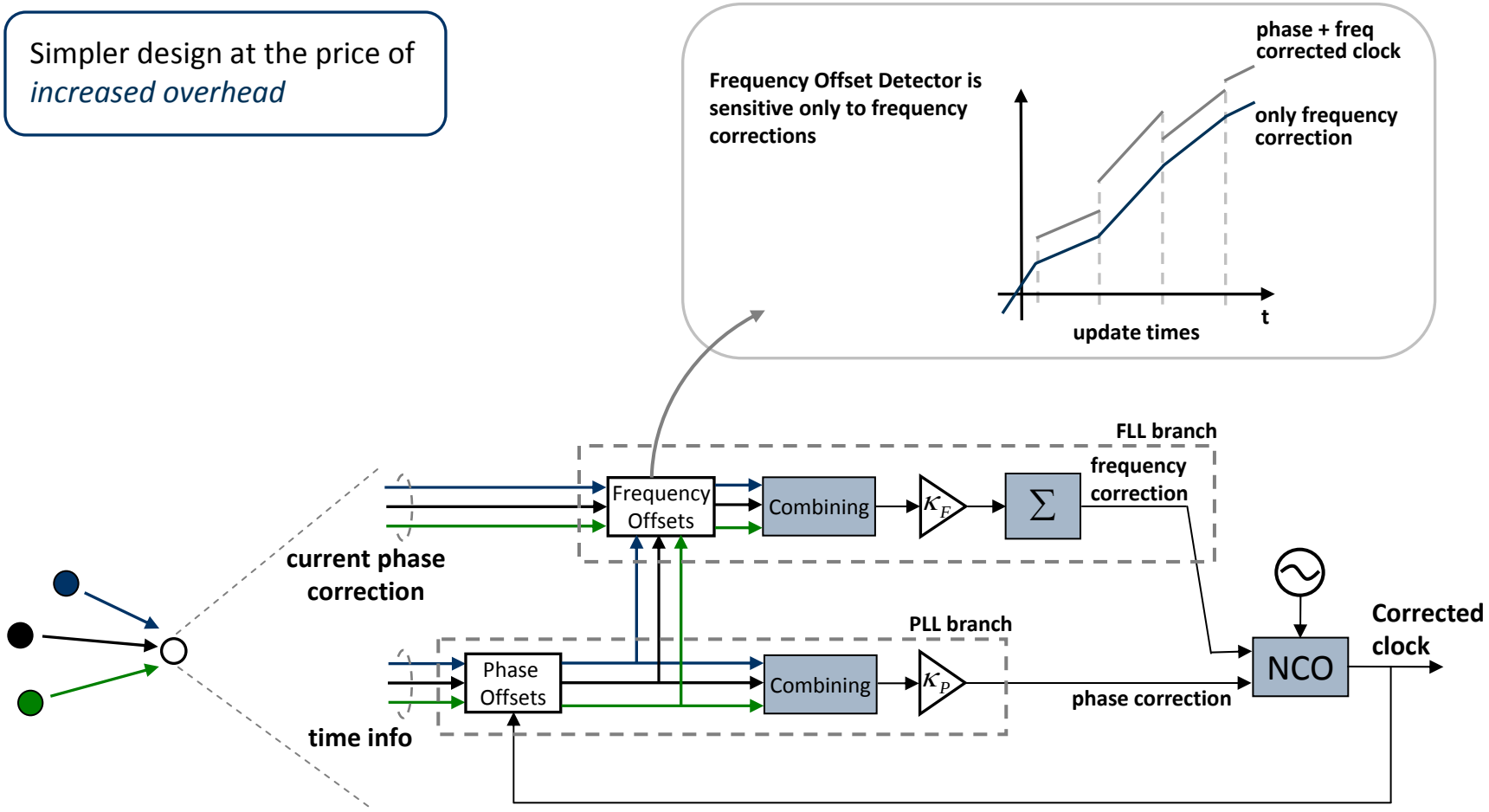
$$\sigma^2(T_{SF}) = E\left[\left|\alpha(nT_{SF}) - \alpha((n-1)T_{SF})\right|^2\right]$$

- *proposed solution*: frequency *tracking* via:
  - Type 2 PLL
  - *Type 1 PLL+FLL (P/FLL)*



Type 1 PLL + FLL

Simpler design at the price of *increased overhead*



Tracking - Results

- Closed-form tracking accuracy in *regular* MC networks

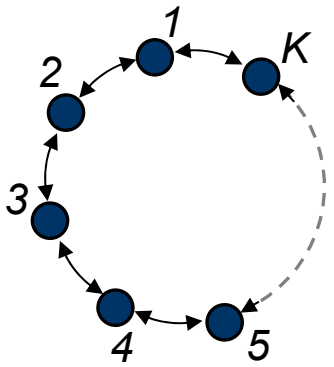
P/FLL $$\xi^2 \simeq \frac{1}{K}\sum_{i=2}^{K}\frac{1}{2\mu_i}\left[\left(\rho+\frac{\gamma}{\rho}\right)\frac{\sigma_w^2}{d}+\frac{\sigma_v^2}{\rho}+\frac{\sigma_\eta^2}{\mu_i^2\gamma\rho}\right]$$

Type 2 PLL $$\xi^2 \simeq \frac{1}{K}\sum_{i=2}^{K}\frac{1}{2\mu_i}\left[\left(\kappa_1+\frac{\kappa_2}{\mu_i}\right)\frac{\sigma_w^2}{d}+\frac{\sigma_v^2}{\kappa_1}+\frac{\sigma_\eta^2}{\kappa_2\kappa_1\mu_i}\right]$$

network connectivity

channel noise (time offset estimation error)

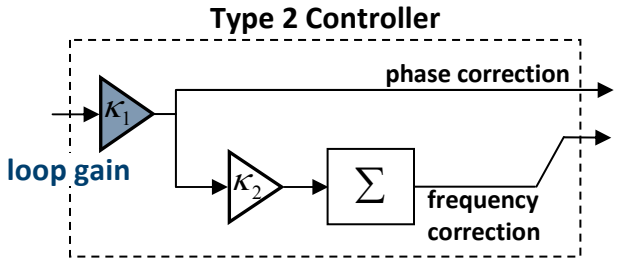
tracking error (WFM + RWFM)



- better connectivity improves sync accuracy
- trade-off between channel noise reduction and frequency tracking
- integral gain κ_2 proportional to loop gain κ_1 :
  - small κ_1 improves channel noise rejection → previous part
  - *large κ_1 improves tracking accuracy of unstable clocks*

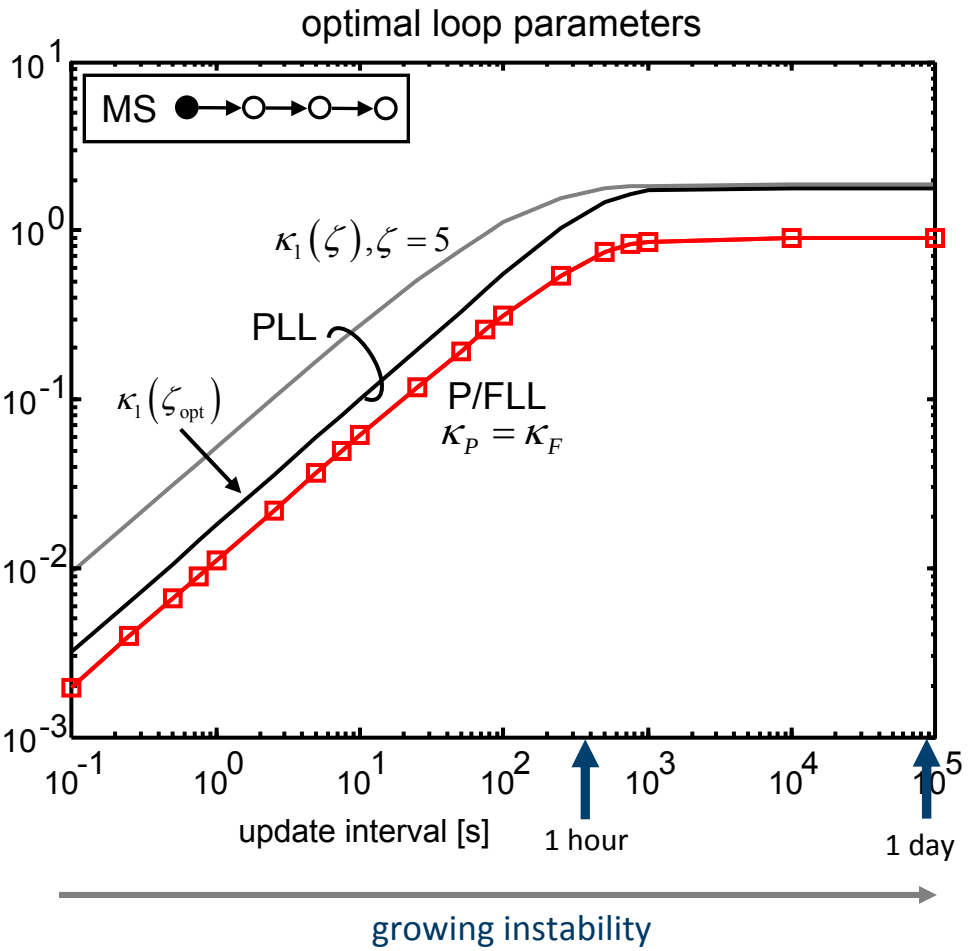
Optimal Parameter Adaptation

- Numerical optimization of loop parameters
  - P/FLL: opt. PLL gain κ_P + opt. FLL gain κ_F
  - PLL: - optimize jointly l.gain/damping
    - fix damping and optimize l.gain



- MS line network of 30 nodes
- 1°C temp change within 1 hour

- gain increases proportionally with clock instability

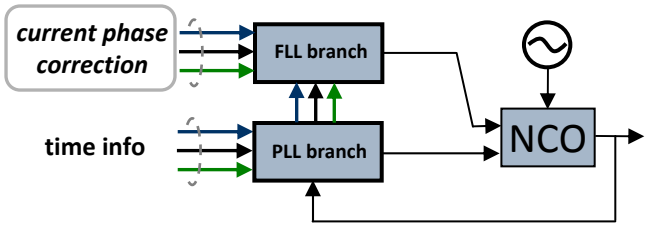


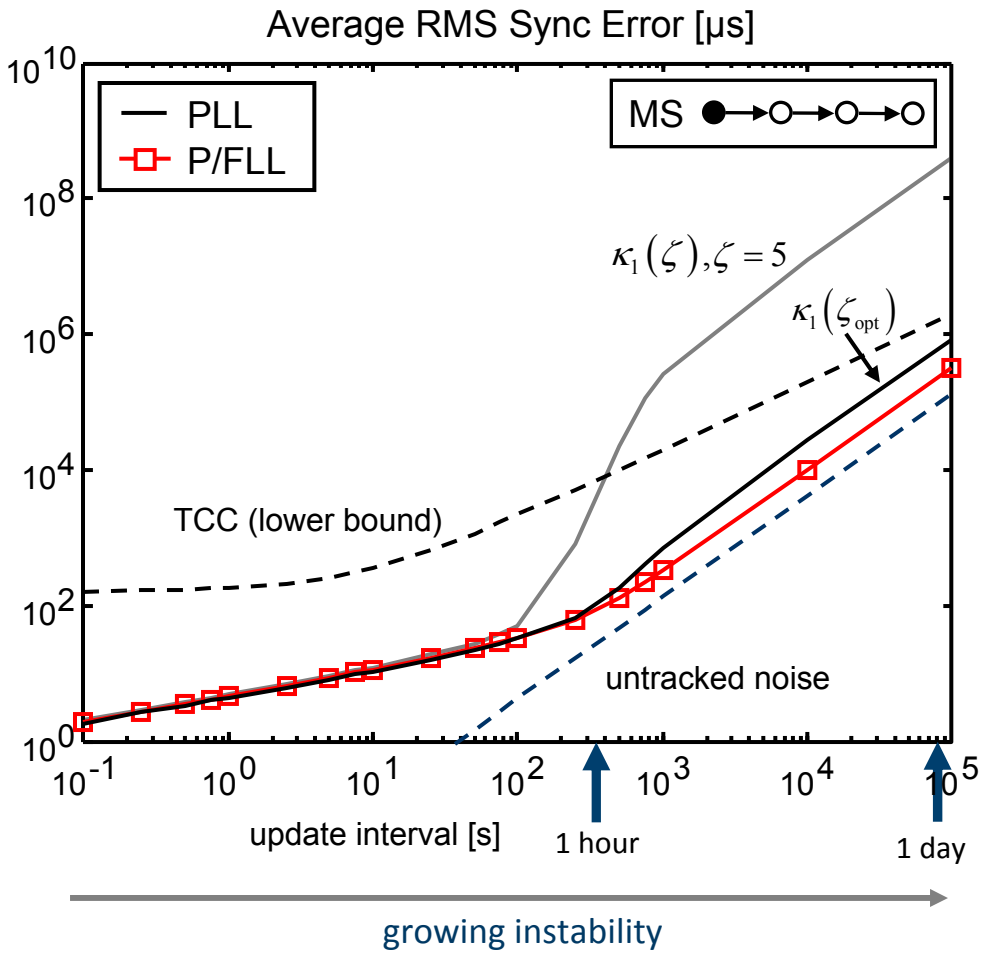
Tracking Performance

- Average synchronization error for a line MS network of 30 nodes
- 1°C temp change per 1 hour

- adaptive clock control outperforms TCC
- adaptation complexity
  - for optimal performance, PLL requires to *jointly* adapt damping and loop gain
  - optimization of PLL and FLL branch is *independent* in a P/FLL

  Simpler design at the price of increased overhead





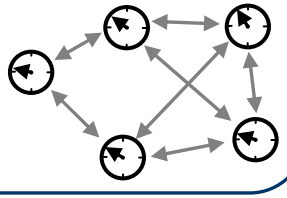
Outline

- Motivation
- Synchronization at the physical layer
- Synchronization at the MAC layer
- Conclusions

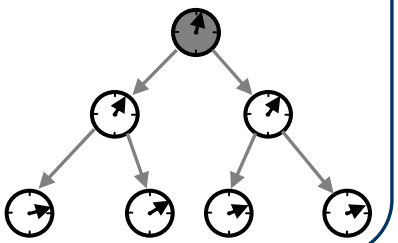
Conclusions

- Advocate network sync via PLL/FLL techniques
  - can be applied at PHY/MAC/APP layer at the protocol stack
    → robust wrt RF *signal superposition* and *packet collisions*
  - general-purpose tool for *both* MS/MC sync architectures
    → allow for improved *sync accuracy* and *tracking* performance
  - can be adapted to large update periods (low duty-cycles) → WSN based on TDMA
- Best flat (MC) or hierarchical (MS) sync architecture ?

MC
+ fully decentralized
+ robust wrt node failures
+ smooth error distribution
- slow convergence



MS
+ natural arch. for hierarchical networks
+ fast convergence
- error accumulation away from master(s)
- fragile to node failures



Conclusions

This seminar: Design of distributed clock control algorithms

Future work:

- Design algorithms that dynamically adapt loop parameters to
  - topology (connectivity)
  - architecture (MS/MC)
  - duty cycles (energy efficient sync)
  - clock quality (frequency instability)
  - channel error statistics
  - → lessons learned from packet-based sync algorithms (NTP)
- Implementation of the designed algorithms
  - improvements to the efficiency of currently employed TDMA MAC protocols (e.g., IEEE 802.15.4e)
  - complexity/computational cost

Conclusions

RELATED PUBLICATIONS

- N. Varanese, U. Spagnolini and Y. Bar-Ness, "*Synchronization tracking with low duty cycles*", in preparation.
- N. Varanese, U. Spagnolini and Y. Bar-Ness, "*On the accuracy of distributed synchronization algorithms for wireless networks*", in preparation.
- N. Varanese, U. Spagnolini and Y. Bar-Ness, "*Distributed frequency-locked loops for wireless networks*", submitted to IEEE Trans. on Communications (*second review round*).
- N. Varanese, Y. Bar-Ness and U. Spagnolini, "*On the synchronization rate of distributed medium access protocols*," Proc. Conference on Information Sciences and Systems (CISS) 2010, Princeton, NJ USA, March 17-19, 2010.
- U. Spagnolini, N. Varanese, O. Simeone and Y. Bar-Ness, "*Distributed Digital Locked Loops for time/frequency locking in packet-based wireless communication*," in Proc. IEEE PIMRC 2008, Cannes, France, Sept. 15-18, 2008 (invited paper).
- N. Varanese, O. Simeone, Y. Bar-Ness and U. Spagnolini, "*Distributed Frequency-Locked loops for wireless networks*," in Proc. IEEE ISSSTA 2008, Bologna, Italy, Aug. 25-28, 2008.

Questions ?