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Distributed synchronization algorithms for wireless sensor networks

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Abstract:

The ability to distribute time and frequency among a large population of interacting agents is of interest for diverse disciplines, inasmuch as it enables to carry out complex cooperative tasks. In a wireless sensor network (WSN), time/frequency synchronization allows the implementation of distributed signal processing and coding techniques, and the realization of coordinated access to the shared wireless medium. Large multi-hop WSN's constitute a new regime for network synchronization, as they call for the development of scalable, fully distributed synchronization algorithms. While most of previous research focused on synchronization at the application layer, this lecture considers synchronization at the lowest layers of the communication protocol stack, namely the physical and the medium access control (MAC) layer. At the physical layer, we focus on the compensation of carrier frequency offsets (CFO), while at the MAC layer the focus is on time synchronization. The problem of realizing network-wide synchronization is approached by employing distributed clock control algorithms based on the classical concept of coupled phase and frequency locked loops (PLL, FLL). Our analysis takes into account communication, signaling and energy consumption constraints arising in the novel context of multi-hop WSN's. The robustness of the algorithms is checked against infrequent sync updates and errors introduced by different noise sources, such as transmission delays and clock frequency instabilities. By observing that WSN's allow for greater flexibility in the design of the synchronization network architecture, this lecture examines also the relative merits of peer-to-peer (mutually coupled - MC) and hierarchical (master- slave - MS) architectures. For all the considered cases, synchronization algorithms based on adaptive PLL and FLL designs are shown to provide robust and scalable network-wide time and frequency distribution in a WSN.

Biography:

Nicola Varanese received the M.Sc. degree (with honors) in Telecommunication Engineering from Politecnico di Milano, Milan, Italy, in 2006, the Ph.D. degree in Electrical Engineering from New Jersey Institute of Technology, Newark, NJ, and the Ph.D. degree in Information Engineering from Politecnico di Milano in 2011. He is currently with the Dipartimento di Elettronica e Informazione, Politecnico di Milano, where he is a research assistant. His current research interests include the analysis and design of wireless sensor networks with emphasis on synchronization and resource allocation issues.