Distributed Synchronization Algorithms for Wireless Sensor Networks

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Outline

- Motivation
- Synchronization at the physical layer
- Synchronization at the MAC layer
- Conclusions
Synchronization is the simplest form of cooperation and enables more complex cooperative tasks

- Communication Networks:
  synchronization at different layers

- Network Time Protocol - NTP (v3 1991, v4 in draft)
- Industrial Ethernet (EtherCAT), digital cellular systems – timing advance for TDMA (1990’s)
- TDM circuit-switched carrier networks (1970’s - 1980’s)
Synchronization is the simplest form of cooperation and enables more complex cooperative tasks.

- Communication Networks:
  synchronization at different layers

Timing packets:
- Software PLL (linear clock control)
- Kalman tracking
- estimation of clock parameters (phase/frequency/drift)
- other (e.g., nonlinear clock correction)

Electrical/RF signals:
- Analogue Phase-locked Loop (APLL)
- (All) Digital PLL (DPLL)
- analogue/digital Frequency-locked Loop (FLL)
Synchronization is the simplest form of cooperation and enables more complex cooperative tasks.

- **Wireless Sensor** Networks: synchronization at different layers.

**Motivation**

- **Physical** communication
  - Cooperative communication
  - Time offset
  - Information blocks
  - Distributed space-time code
  - ISI
  - Received block
Motivation

Synchronization is the simplest form of cooperation and enables more complex cooperative tasks.

- **Wireless Sensor** Networks: synchronization at different layers.

MAC: coordinated medium access

![Diagram showing synchronization and collisions in different layers](image-url)
Motivation

Synchronization is the simplest form of cooperation and enables more complex cooperative tasks.

- **Wireless Sensor Networks:** synchronization at different layers

Application: distributed sensing

- $p(x,y;t)$
  - $x$
  - $y$
Focus of Major Research Topic

Synchronization is the simplest form of cooperation and enables more complex cooperative tasks

- **Wireless Sensor** Networks: synchronization at different layers

  - APP
  - NET
  - MAC
  - PHY

  2002

  2010

  most of prior art

  time synchronization

  carrier frequency offset (CFO) compensation

  RF Transceiver

  MCU

  software processes
Approach: Clock Control

- Prior Art:
  - estimation of clock parameters [Kumar08][Estrin04]
  - distributed agreement (consensus) algorithms [Simeone07][Schenato09]

- Our approach:
  - control of the local clock
  - via Phase and Frequency-Locked Loops (PLL, FLL)

PLL is the classical approach for wired networks (TDM, NTP, PTP)

*what about wireless?*
Approach: Clock Control

- Prior Art:
  - estimation of clock parameters
  - distributed agreement algorithms

- Our approach:
  control of the local clock
  via Phase and Frequency-Locked Loops (PLL, FLL)

- Challenges:
  - superposition of radio signals
  - packet collisions
  - energy constraints (low duty cycles)
Approach: Sync Topologies

- **WSN** offer wider flexibility in sync architecture design

- **Prior Art:**
  - *specific* tools for each sync topology, e.g.
    - MS: linear regression (FTSP [Maróti04])
    - MC: distributed consensus (ATS [Schenato09])

- **Our approach:**
  PLL/FLL as a *distributed* clock control tool suitable for *any* sync topology

master-slave (MS): hierarchical

mutually coupled (MC): peer-to-peer

hybrid
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- Synchronization at the physical layer
  - distributed compensation of Carrier Frequency Offsets (CFO)

- Synchronization at the MAC layer

- Conclusions
Distributed CFO Correction

- Sync preamble for CFO estimation
- CFO correction via *distributed-FLL* (D-FLL)
- design of novel Frequency Difference Detector (FDD)
  - *superposition* of preamble signals
  - based on sample auto-correlation
  - nonlinear characteristic

- analysis:
  - frequency *acquisition* (stability and conv. speed)
  - steady-state sync *accuracy*
Frequency Acquisition

- frequency acquisition
  - FDD locking range
  - stability conditions (MC networks)
    - connectivity
    - mutual interference

- comparison with DFT-based FDD for a simple MC network

![Graph showing Average RMS CFO (norm. freq.) vs iterations for DBQC and DFT-based methods with different symbols (L=5, L=21).]
Frequency Tracking

- Steady-state sync accuracy
  - channel noise and frequency instability (WFM)
  - MC and MS topologies

- residual CFO distribution in a MC and MS line network

- FLL bandwidth tuned via loop gain $\varepsilon$

![Diagram](image)

- RMS CFO (norm. freq.)

- MC
- MS

- $\varepsilon = 1$
- $\varepsilon = 0.9$
- $\varepsilon = 0.3$

![Graph](image)
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  - Convergence rate of distributed sync algorithms
  - Steady-state sync accuracy
  - Sync tracking with low duty-cycles
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Super-frame structure

General SF structure for a slotted-access MAC layer:

- **Super-frame**: sync update length period
- **Signaling slot(s)**: beacon slots
- **Data slots**:
- **Time information**:
  - Pulse (frame sync seq.)
  - Time-stamp (hh:mm)
- **Access protocols for signaling slots**
- **NTP/PTP, others**: handshakes
  - **Our case**: broadcast
  - **No timing handshakes**

IEEE 802.15.4/e (ZigBee/SP100)
IEEE 802.11 (Wi-Fi)
ECMA 368 (WiMedia)
Each node employs time info to control the local clock via a PLL:

Analysis of *distributed* PLL:
- time sync *acquisition* (stability and conv. speed)
- steady-state accuracy:
  - *stable* clocks: frequency is constant bw updates
  - *unstable* clocks: frequency changes bw updates

Impact of topology
- MC
- MS

Choice of loop parameters:
- loop gain $\kappa_1$
- damping $\zeta(\kappa_1, \kappa_2)$
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Time Sync Acquisition

Time information:

- pulse (frame sync word) → superposition of pulses
- time-stamp → contention or reservation-based transmission
Time Sync Acquisition - Results

- acquisition trivial for MS \(\rightarrow\) analysis focused on MC networks

- *superposition* and *contention*:
  - almost sure convergence condition: convergence *in the mean*

- *reservation*:
  - overhead of signaling slots
Time Sync Acquisition - Results

- Hp: clocks are frequency synchronous
  - Type 1 PLL for time (phase) sync

- $0 < \varepsilon < 1$ ensures stability
- Numerical optimization of loop gain $\varepsilon$ for a given square lattice topology:

![Diagram of TOD and loop gain](image)

![Graph of Sync Acquisition Time](image)

- Sync Acquisition Time [sig. slots]
  - Superposition
  - Contention
  - Reservation
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Synchronization Accuracy

- TDMA MAC protocol
  - reservation-based signaling

- Hp: clk frequency is stable
  - linear clock model

- sync accuracy depends on pair-wise offset estimation errors.
  - delivery delays
  - clock precision (quantization)

- network sync posed as a (distributed) linear regression problem
  - distributed type 2 PLL
  - distributed linear regression (DLR)
  - \( Cramér–Rao lower bound \)
Cramér–Rao Lower Bound

- CRLB: lower bound to clock parameter estimation error
  - linear clock model: estimate phase and frequency
  - time offset observations from signaling slots of subsequent super-frames
  - centralized block-estimation model:

\[ T_k(t) = \alpha_k t + \beta_k \]

\( (\text{absolute time}) \)

\[ \xi_{p,f}^2 \geq \rho_{p,f} \cdot \frac{1}{K} \sum_{i=1}^{K} \frac{1}{\mu_i} \]

CRLB for a general topology

CRLB for linear regression of phase/frequency

sync network architecture

Training

\( N \text{ super-frames} \)
CRLB : MS Vs MC

- Cramér–Rao lower bound for general sync architectures (MS, MC, hybrid)
  - MC: error distributed almost uniformly
  - MS: error distributed inhomogeneously - accuracy degrades rapidly moving away from masters

- CRLB for 2D 30x30 square lattice deployment (in $\mu$s)
  (Gaussian offset measurement error with 10$\mu$s std dev, N=10)
Distributed Linear Regression

- Design of *Distributed linear regression* (DLR) algorithm
  - linear clock model: estimate phase and frequency
  - time translation: \( t = \frac{T_k(t) - \beta_k}{\alpha_k} \)
  - signaling slots employed for training and *distributed fusion*

\[ T_k(t) = \alpha_k t + \beta_k \]
Type 2 PLL

- PLL clock control
  - linear clock model → linear clock control
  - PI (type 2) controller: phase and frequency control
  - provides a prediction of the start time of next super-frame wrt local clock

\[ T_{SF} = \text{sync update} \]

\[ \alpha_k T_{SF} \]

\[ T_k(nT_{SF}) : \text{start of next super-frame wrt node k's clock} \]
Lessons Learned

- DLR: closed-form sync accuracy for general networks
- PLL: closed-form sync accuracy for regular MC networks

*Effective* samples for PLL algorithms [Mengali94]

\[
N_{\text{eff}} = \frac{2}{\frac{\kappa_1}{2} \left( 1 + \frac{\kappa_2}{\kappa_1} \right)}
\]

- Regular topology: *ring network*
  - CRB accuracy limit
    \[
    \xi^2_{\text{CRB}} \approx \frac{2\sigma_w^2}{N_{\text{eff}}} \frac{1}{\mu_2}
    \]
  - DLR accuracy
    \[
    \xi^2_{\text{DLR}} \approx \frac{4d\sigma_w^2}{N_{\text{eff}}} \frac{1}{\mu_2}
    \]
  - PLL accuracy
    \[
    \xi^2_{\text{PLL}} \approx \frac{4d\sigma_w^2}{N_{\text{eff}}} \frac{1}{\mu_2} \frac{1}{1 + 4\xi^2}
    \]

- Better connectivity improves accuracy
- Improved noise filtering
Accuracy of MC Networks

- Accuracy of practical algorithms over MC networks
- Line network of 31 nodes, N=1000
- Sub-optimality of both PLL and DLR wrt CRB
  - Price to pay for broadcast signaling

![Diagram showing RMS Sync Error vs Node index with graphs for PLL, DLR, and CRB]
PLL: MC Vs MS

- Fix a desired time (phase) sync accuracy $\xi$
  - MC: accuracy improves *increasing transmission range*
  - MS/Hybrid: accuracy improves increasing transmission range or *master node density*

- MS/Hybrid: for a given transmission range, *how many master nodes do I need?*

- Line network of 31 nodes, $N=1000$

- MC accuracy rapidly improves with transmission range

![Graph](image-url)

- Number of Master nodes against transmission range (norm.)
  - $\xi = 1\mu s$
  - $\xi = 500\mu s$

N. Varanese, Distributed Synchronization 02/10/2011
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Sync Tracking with Low Duty-Cycles

- TDMA MAC protocol
  - reservation-based signaling

- low duty cycle → infrequent sync updates
  - clock is unstable: temp. changes

- current solution: static temp. compensation (Temp. Compensated Clock - TCC)

- achievable accuracy (lower bound for MS)

\[ \xi = 2\alpha_{\text{max}} T_{SF} + \delta \]

- residual frequ. offset
- phase offset estimation accuracy

\[ \alpha_{\text{max}} \]

\[ T_{SF} \]

\[ \delta \]

**super-frame** = sync update

**active period**

**idle period**

**frequency offset [ppm]**

**°C**

**TCC** [Pister ‘07]

**tuning-fork XO**

**-160**

**40**

**90**

**0**

**-40**

**-25**
Model of an Unstable Clock

- **Hp**: clock frequency is the sum of two indep. random processes
  \[ \alpha(nT_{SF}) = \bar{\alpha} + \nu(nT_{SF}) + \psi(nT_{SF}) \]
  - random walk (RWFM)
  - white noise (WFM)

- **WFM**: noise within the oscillator
- **RWFM**: temperature changes, mechanical shocks and vibrations

- **Allan Variance**: a measure of frequency stability
  \[ \sigma^2(T_{SF}) = E \left[ \alpha(nT_{SF}) - \alpha((n-1)T_{SF}) \right]^2 \]

- **proposed solution**: frequency tracking via:
  - Type 2 PLL
  - **Type 1 PLL+FLL (P/FLL)**

\[ T_{SF} = \text{sync update} \]

\[ (n-1)T_{SF} \quad nT_{SF} \]

**Diagram**:
- \[ \log \sigma(T_{SF}) \]
- WPM
- WFM \( \propto \frac{1}{T_{SF}} \)
- RWFM \( \propto T_{SF} \)

**Graph**: nice spot! (Allan intercept)
- weak instability
- strong instability
Type 1 PLL + FLL

Simpler design at the price of increased overhead.
Tracking - Results

- Closed-form tracking accuracy in regular MC networks

\[ \xi^2 \approx \frac{1}{K} \sum_{i=2}^{K} \frac{1}{2\mu_i} \left[ \left( \rho + \frac{\gamma}{\rho} \right) \frac{\sigma_w^2}{d} + \frac{\sigma_v^2}{\rho} + \frac{\sigma_\eta^2}{\mu_i^2 \gamma \rho} \right] \]

Type 2 PLL

\[ \xi^2 \approx \frac{1}{K} \sum_{i=2}^{K} \frac{1}{2\mu_i} \left[ \left( \varsigma_1 + \frac{\varsigma_2}{\mu_i} \right) \frac{\sigma_w^2}{d} + \frac{\sigma_v^2}{\varsigma_1} + \frac{\sigma_\eta^2}{\varsigma_2 \varsigma_1 \mu_i} \right] \]

- better connectivity improves sync accuracy

- trade-off between channel noise reduction and frequency tracking

- integral gain \( \varsigma_2 \) proportional to loop gain \( \varsigma_1 \):
  - small \( \varsigma_1 \) improves channel noise rejection
  - large \( \varsigma_1 \) improves tracking accuracy of unstable clocks
Optimal Parameter Adaptation

- Numerical optimization of loop parameters
  - P/FLL: opt. PLL gain $\kappa_p +$ opt. FLL gain $\kappa_f$
  - PLL: - optimize jointly l.gain/damping
    - fix damping and optimize l.gain

- MS line network of 30 nodes
- 1°C temp change within 1 hour
- gain increases proportionally with clock instability

![Diagram of Type 2 Controller with phase and frequency corrections]

**optimal loop parameters**

- $\kappa_1(\zeta), \zeta = 5$
- $\kappa_1(\zeta_{opt})$

$\kappa_P = \kappa_F$

![Graph showing optimal loop parameters over update interval from 1 hour to 1 day]

Growing instability
Tracking Performance

- Average synchronization error for a line MS network of 30 nodes
- 1°C temp change per 1 hour

- adaptive clock control outperforms TCC
- adaptation complexity
  - for optimal performance, PLL requires to jointly adapt damping and loop gain
  - optimization of PLL and FLL branch is independent in a P/FLL
    Simpler design at the price of increased overhead
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Conclusions

- Advocate network sync via PLL/FLL techniques
  - can be applied at PHY/MAC/APP layer at the protocol stack
    - robust wrt RF signal superposition and packet collisions
  - general-purpose tool for both MS/MC sync architectures
    - allow for improved sync accuracy and tracking performance
  - can be adapted to large update periods (low duty-cycles) WSN based on TDMA

- Best flat (MC) or hierarchical (MS) sync architecture?

MC
- fully decentralized
- robust wrt node failures
- smooth error distribution
- slow convergence

MS
- natural arch. for hierarchical networks
- fast convergence
- error accumulation away from master(s)
- fragile to node failures
Conclusions

This seminar: Design of distributed clock control algorithms

Future work:

• Design algorithms that dynamically adapt loop parameters to
  ▪ topology (connectivity)
  ▪ architecture (MS/MC)
  ▪ duty cycles (energy efficient sync)
  ▪ clock quality (frequency instability)
  ▪ channel error statistics
  → lessons learned from packet-based sync algorithms (NTP)

• Implementation of the designed algorithms
  ▪ improvements to the efficiency of currently employed TDMA MAC protocols
    (e.g., IEEE 802.15.4e)
  ▪ complexity/computational cost
Conclusions

RELATED PUBLICATIONS


Questions ?